Page 26, strike all of line 6, and substitute the following therefore: --Harari, Serial No. 07/337,579, filed April 13, 1989, now abandoned,--

Page 32, between lines 20 and 21, in the text added by the Preliminary Amendment filed December 20, 1996:

(1) Page 10, line 26, after "204,175," insert --now patent no. 5,095,344,--;

(2) Page 13, line 16, after "204,175," insert --now patent no. 5,095,344,--; and

(3) Page 13, line 33, change "204,175" to --204,175, now patent no. 5,095,344,--.

IN THE CLAIMS:

Please amend claims 63-70 as follows:

63. (Amended) A method of operating an EEprom system having memory cells that individually include an electrically floating gate carrying a charge level that is alterable in response to appropriate [voltages] voltage conditions being applied to the cell[, thereby] in order to [establish] set a variable threshold level that is [detectable upon] determinable by reading the cell to be in one of at least two defined threshold level regions, said method comprising:

applying said appropriate [voltages] voltage conditions to a plurality of said memory cells in parallel, thereby to alter the charge levels on the floating gates of said plurality of memory cells,

[individually detecting] determining the threshold [levels] level regions of individual ones of said plurality of memory cells, and

terminating said application of appropriate [voltages] voltage conditions to individual ones of said plurality of memory cells [as soon as they are detected] upon their being determined to have reached desired ones of said at least two threshold [levels] level ranges while continuing to apply said appropriate [voltages] voltage conditions to others of said plurality of cells until all of the plurality of cells are [detected] determined to have reached desired ones of said at least two threshold [levels] level ranges.

64. (Amended) The method of claim 63, wherein there are exactly two of said [desired] defined threshold [levels] level ranges.

65. (Amended) The method of claim 63, wherein there are more than two of said [desired] defined threshold [levels] level ranges.

66. (Amended) The method of claim 63, wherein said [desired] at least two threshold level ranges [levels of the plurality of memory cells include] are separated by exactly one breakpoint threshold level, thereby to provide exactly two non-overlapping [programmed ranges of] threshold [levels] level ranges.

67. (Amended) The method of claim 63, wherein said [desired] at least two threshold level ranges [levels of the plurality of memory cells include] are separated by more than one breakpoint threshold level, thereby to provide more than two non-overlapping [programmed ranges of] threshold [levels] level ranges.

68. (Amended) The method of claim 63, wherein said [desired] at least two defined threshold [levels] level ranges include an erased threshold level.

69. (Amended) The method of claim 63, wherein the array of memory cells are grouped into blocks of cells [whose] wherein the threshold levels of cells within a selected one of the blocks are changed together to a single given level prior to applying [the] said appropriate [voltages] voltage conditions in parallel to the plurality of cells within said one block.

70. (Amended) The method of claim 69, wherein said plurality of memory cells to which said appropriate [voltages] voltage conditions are applied in parallel are less than a number of memory cells within individual ones of said blocks, and additionally comprising repeating for another plurality of cells within said one [of said blocks] block said applying, [detecting] determining and terminating operations.

Please add the following new claims:

--73. The method of claim 63, wherein the array of memory cells are grouped into blocks of cells wherein the threshold levels of cells within individual ones of the blocks are changed together to a single given level prior to applying said appropriate

voltage conditions in parallel to the plurality of cells within one of the blocks, the method further comprising simultaneously changing the cells of a selected two or more blocks to said given level.

74. The method of either of claims 70 or 73, wherein said single given level is within one of said at least two defined threshold level regions.

75. The method of claim 63 wherein the desired ones of at least two threshold level ranges reached by applying appropriate voltage conditions to the plurality of memory cells correspond to a chunk of input data being programmed into the memory system.

76. The method of claim 75, wherein the plurality of cells are determined to have reached the desired ones of said at least two threshold level ranges by comparing the threshold levels of the plurality of cells with the chunk of input data.

77. The method of claim 76, wherein the chunk of input data is stored in a cache memory prior to being programmed into the memory system.

~~78~~ 75. The method of claim ~~67~~, wherein the appropriate voltage conditions are applied to said plurality of memory cells in successive applications of said voltage pulses that individually shift the threshold level of the cells to which the voltage pulses are applied less than one half of a difference between adjacent ones of the breakpoint levels.

79. The method of either of claims 65 or 67, wherein terminating the application of appropriate voltage conditions to individual ones of the plurality of memory cells occurs upon their being determined to have been programmed to within the desired ones of said at least two threshold levels by a margin.

~~80~~ 78. The method of any one of claims ~~63~~ 1, ~~64~~ 2 or ~~66~~ 4, wherein individual ones of the plurality of memory cells are determined to have reached their desired threshold level ranges by comparison with at least one reference level stored in at least one of the memory cells.

81. The method of either of claims 65 or 67, wherein individual ones of the plurality of memory cells are determined to have reached their desired threshold level ranges by comparison

with two or more reference levels stored two or more of the memory cells.

1982. An electrically erasable and programmable read only memory system, comprising:

an array of electrically alterable memory cells that individually include a field effect transistor having a floating gate and a threshold level that is variable in accordance with an amount of charge carried by the floating gate, said array being divided into blocks of cells that are resettable together, cells within said blocks being addressable for application of programming voltage conditions to individually program them into one of more than two distinct threshold level ranges corresponding to more than one bit of input data per cell,

a reset circuit that simultaneously applies reset voltage conditions to the cells within individual blocks to drive the effective threshold levels of such cells to a reset state,

a programming circuit that applies the programming voltage conditions to a plurality of addressed cells within a reset block to drive the effective threshold voltage of the addressed cells toward one of the more than two programmable threshold level ranges,

a reading circuit that monitors in parallel the threshold level ranges of the plurality of addressed cells, and

a control circuit that individually terminates application of the programming voltage conditions to any one of the plurality of addressed cells when the reading circuit verifies that said any one cell has reached the programmable threshold level range that corresponds to the input data being stored therein, while enabling further application of the programming voltage conditions to others of the plurality of addressed cells that have not yet been so verified, until all of the plurality of addressed cells are verified.

83. The memory system according to claim 82, wherein the plurality of addressed cells are less that a number of cells within the individual blocks.

2184. The memory system according to claim 1982, wherein the control circuit includes a plurality of latches and means for

setting individual ones of the latches in response to corresponding ones of said plurality of addressed cells being verified.

22 ~~85~~. The memory system according to claim 19 ~~82~~, wherein said more than two distinct threshold level ranges are non-overlapping and separated from each other by two or more breakpoint threshold levels.

23 ~~86~~. The memory system according to claim 22 ~~85~~, wherein the reading circuit includes means for ascertaining the individual threshold level ranges of the plurality of memory cells after the cells have been programmed into the individual threshold level ranges beyond one of their breakpoints by a margin.

24 ~~87~~. The memory system according to claim 19 ~~82~~, wherein the programming circuit causes the plurality of addressed cells to be programmed with successive applications of said programming voltage conditions, and the reading circuit operates to monitor the threshold level ranges of the plurality of addressed cells in between applications of said programming voltage conditions.

B cont. 25 ~~88~~. The memory system according to claim 24 ~~87~~, wherein the programming circuit further shifts the threshold levels of the individual addressed cells by less than one half of a difference between at least two breakpoint threshold levels defining one of the threshold level ranges.

26 ~~89~~. The memory system according to claim 24 ~~87~~, wherein the programming circuit further operates with programming voltage conditions that requires a plurality of said successive applications of programming voltage conditions in order to change individual ones of the plurality of addressed cells from one of the threshold level ranges to another adjacent threshold level range.

27 ~~90~~. The memory system according to claim 19 ~~82~~, wherein the control circuit includes a comparator receiving the monitored threshold level range of the plurality of addressed cells and the input data being programmed into the plurality of addressed cells for verifying when the individual ones of the plurality of cells reach the programmable threshold level that corresponds to the input data being stored therein.

28 ~~91~~. The memory system according to claim 19 ~~82~~, wherein at least one reference cell is included in individual ones of the

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blocks of cells, and which additionally comprises means for programming said at least one reference cell to a reference level, and wherein said reading circuit includes means for reading the reference level of the reference cell of the block wherein the plurality of addressed cells exists to verify that any one cell has reached the desired threshold level range.

29 ~~92~~. The memory system according to claim 19 ~~82~~, wherein the reset circuit includes means operable after application of the reset voltage conditions to an addressed at least one block for adjusting to the reset state any cells of said at least one block that were overerased by the reset voltage condition application.

30 ~~93~~. The memory system according to claim 19 ~~82~~, wherein the reset circuit includes means for selecting one or more of the blocks for erase, and means responsive to the selection means for simultaneously applying the reset voltage condition to the memory cells within all of the selected blocks.

31 ~~94~~. The memory system according to claim 30 ~~93~~, wherein the block selecting means includes a register associated with individual ones of the blocks for containing an indication whether the associated block is to be erased.

95. A method of storing a chunk of binary data in an array of integrated circuit non-volatile memory cells which individually have more than two programmable states, comprising:

addressing a plurality of said memory cells sufficient in number to store the chunk of binary data,

applying electrical programming parameters in parallel to the addressed cells,

monitoring the states in which the addressed cells are individually programmed, and

terminating application of programming parameters to individual ones of said addressed cells when they are monitored to have reached desired ones of said more than two programmable states corresponding to the chunk of data being stored, while continuing to apply said programming parameters to others of the addressed cells, until all of the addressed cells are determined to have reached their programmable states corresponding to the chunk of data being stored.

96. The method of claim 95, wherein, prior to applying electrical programming parameters to the addressed cells, at least the addressed cells are all reset to a common state different than either of said more than two programmable states.

97. The method of claim 95, wherein, prior to applying electrical programming parameters to the addressed cells, at least the addressed cells are all reset to one of the more than two programmable states.

98. The method of claim 97, wherein resetting at least the addressed cells includes initially driving at least all of the addressed cells to a common state different than any of said more than two programmable states, and then programming all of at least the addressed cells into said one of the more than two programmable states by the following:

applying electrical programming parameters in parallel to at least the addressed cells,

monitoring the states in which at least the addressed cells are individually programmed, and

terminating application of programming parameters to individual ones of at least the addressed cells when they are monitored to have reached said one of the more than two programmable states while continuing to apply said programming parameters to others of the addressed cells until all of the addressed cells are determined to have reached the reset one of the more than two programmable states.

99. An electrically erasable and programmable non-volatile memory system, comprising:

an integrated circuit array of electrically alterable memory cells that are individually programmable into more than two states, thereby individually storing more than one bit of binary data,

a programming circuit that applies appropriate programming parameters in parallel to an addressed plurality of cells,

a reading circuit that verifies in parallel the state into which the addressed plurality of cells are programmed,